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LHCb Muon Trigger

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1. **Introduction**
2. **Algorithm**
3. **Performance**
4. **Implementation**
5. **Conclusion**

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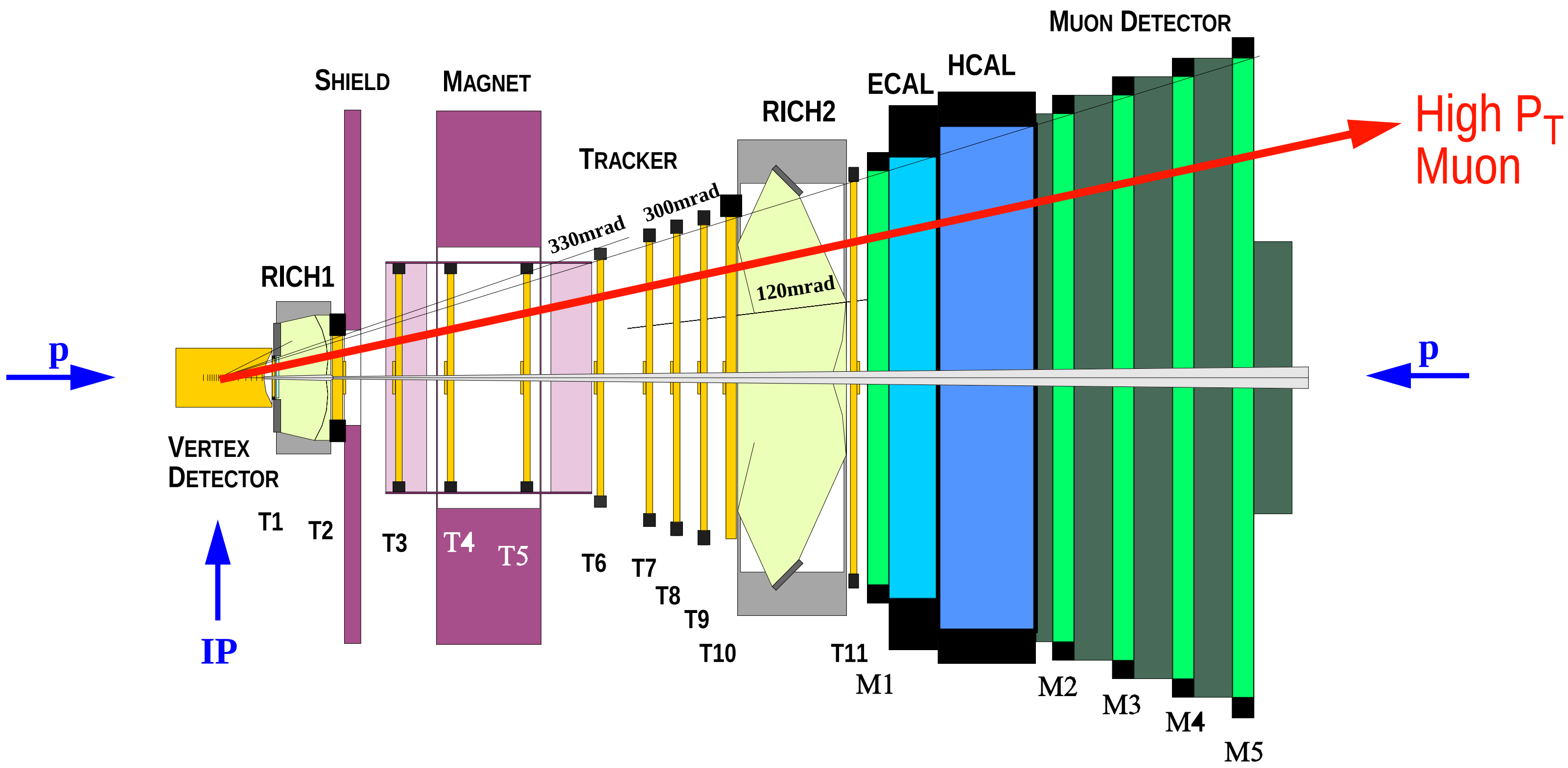
INTRODUCTION

Physics motivation for the muon trigger:

- **Selects efficiently channels of interest:**
  - $B_d \rightarrow J/\psi(\mu^+\mu^-)K_S$
  - $B_s \rightarrow J/\psi(\mu^+\mu^-)\phi$
  - $B_s \rightarrow \mu^+\mu^-$, $B_{s,d} \rightarrow K^{*0}\mu^+\mu^-$
  - ...
- **Selects generic** $B \rightarrow \mu X$ **events**
  - **muon tag**

INTRODUCTION...

- The Muon trigger uses information from all the 5 Muon stations



INTRODUCTION...

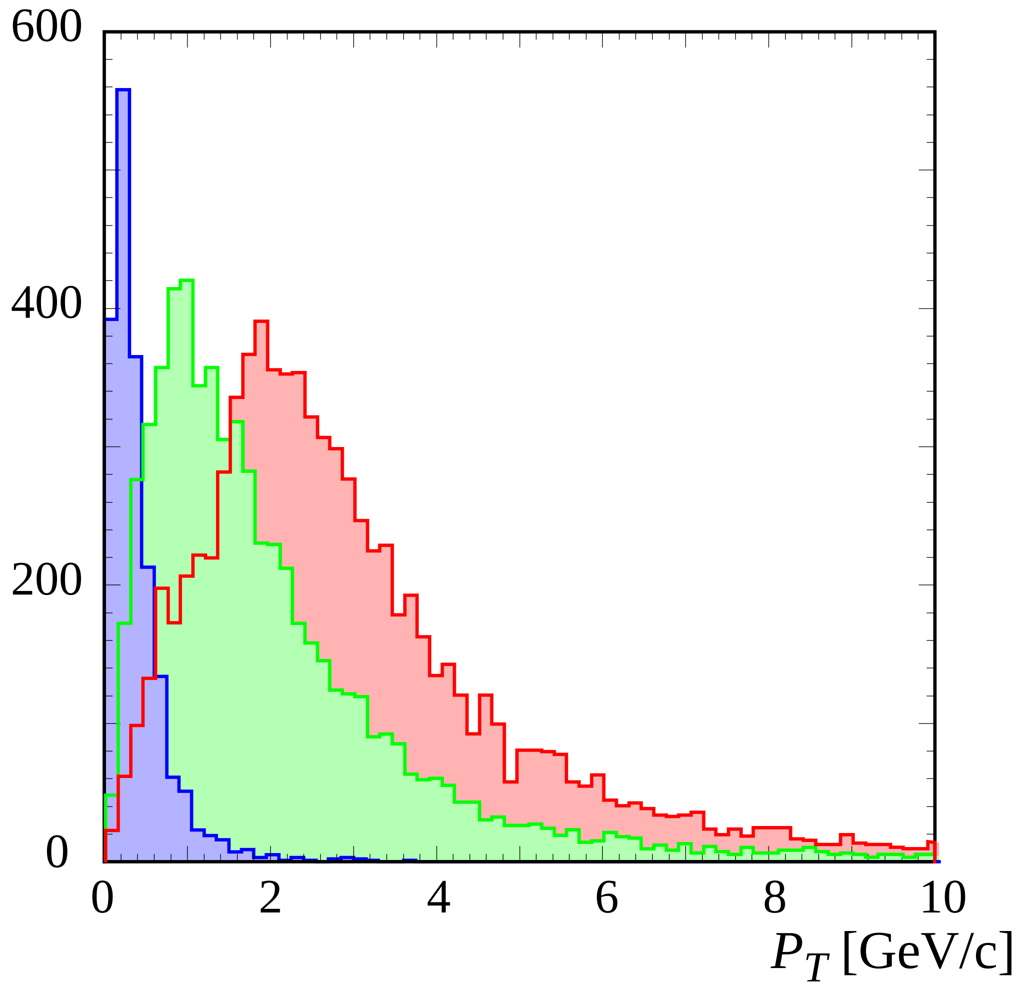
- **The Muon trigger uses information from the Muon system. The Muon trigger identifies muons in the event and measures their transverse momentum P_T**

P_T of the muons hitting the Muon system:

Muons in Minimum bias events: π's and K's decaying in flight

Muons from $B \rightarrow \mu X$ decays

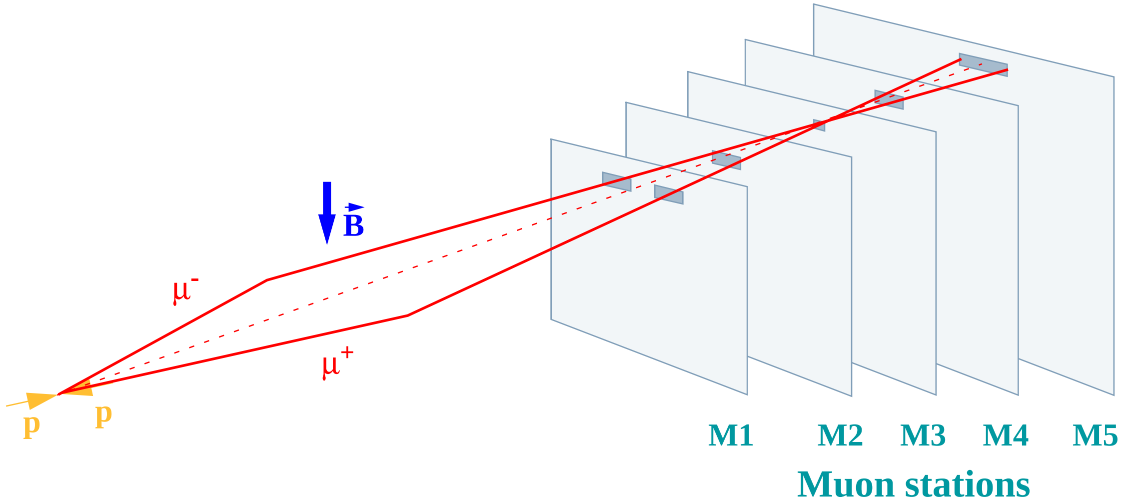
Highest P_T muon in $B_d \rightarrow J/\psi(\mu^+\mu^-)K_S$



ALGORITHM: MUON TRACK FINDING

Find muon track candidate

- Find a seed pad hit in station M3
- Find pads within opened search windows in stations M2, M4, M5
- Use pads found in stations M2 and M3 to extrapolate to station M1
- Find a pad within the opened search window in station M1



Muon trigger exploits multiple scattering in the matter of the Muon shield by applying tight search windows while muon track finding.

ALGORITHM: APPLYING P_T CUT

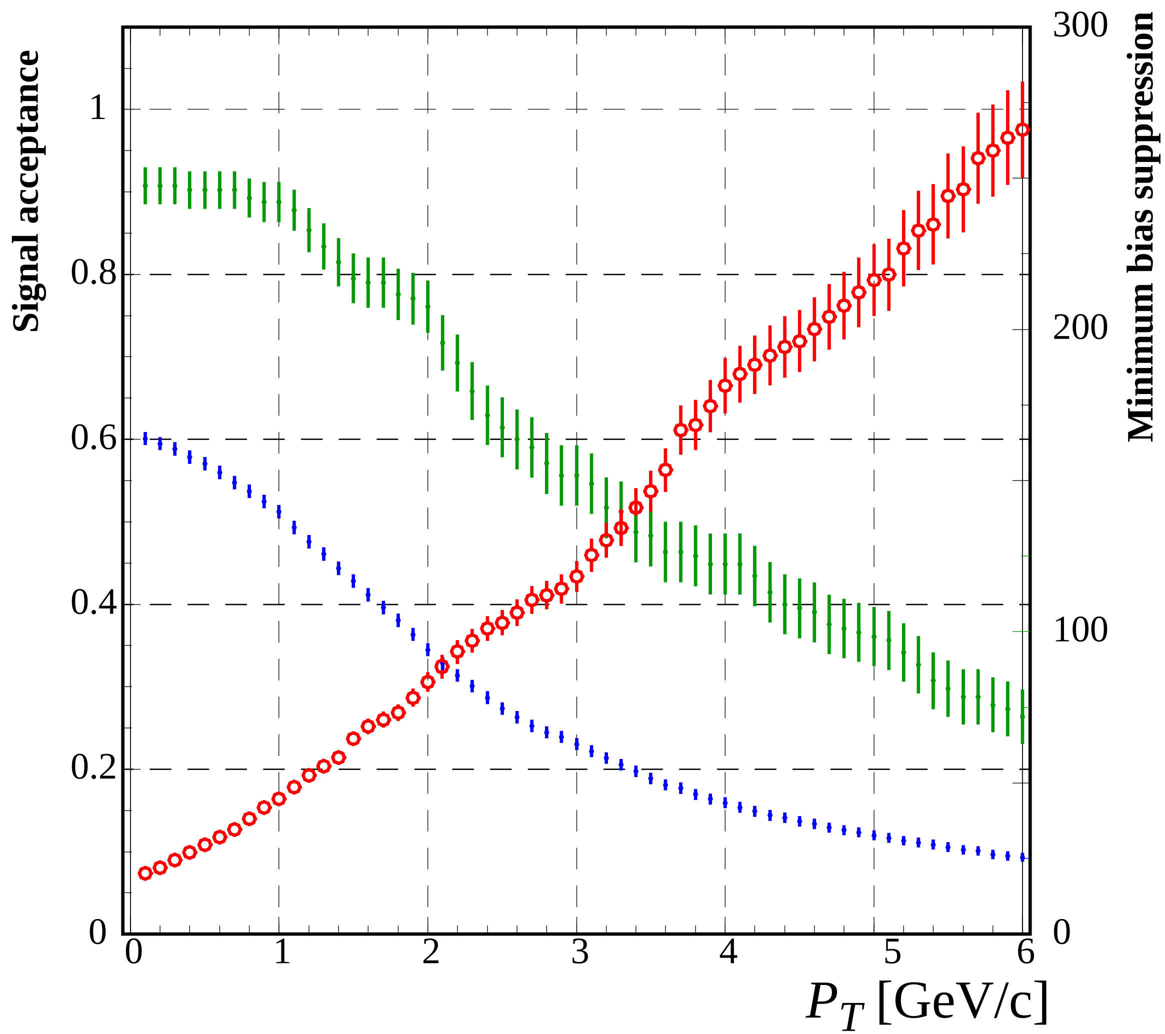
Calculate P_T of the muon candidate from the pad positions in M1 and M2

Pt resolution plot

→ **Approximately equal contributions of the Muon chambers precision and multiple scattering in the calorimeters to the P_T resolution**

PERFORMANCE...

Efficiency

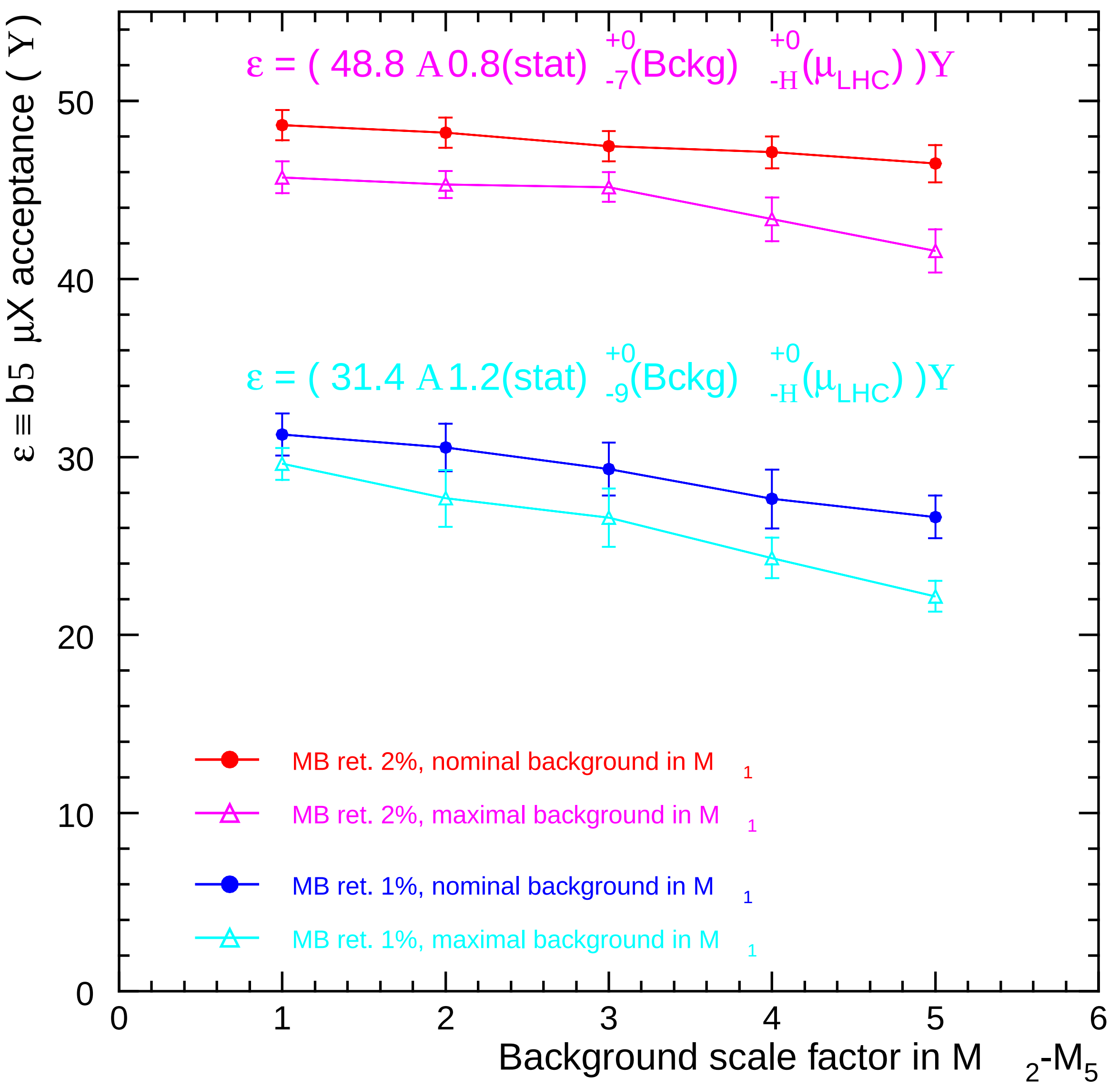


The Muon trigger ensures Minimum bias event suppression factor 50-100

➥ **10 - 20% of the L0 total bandwidth**

PERFORMANCE...

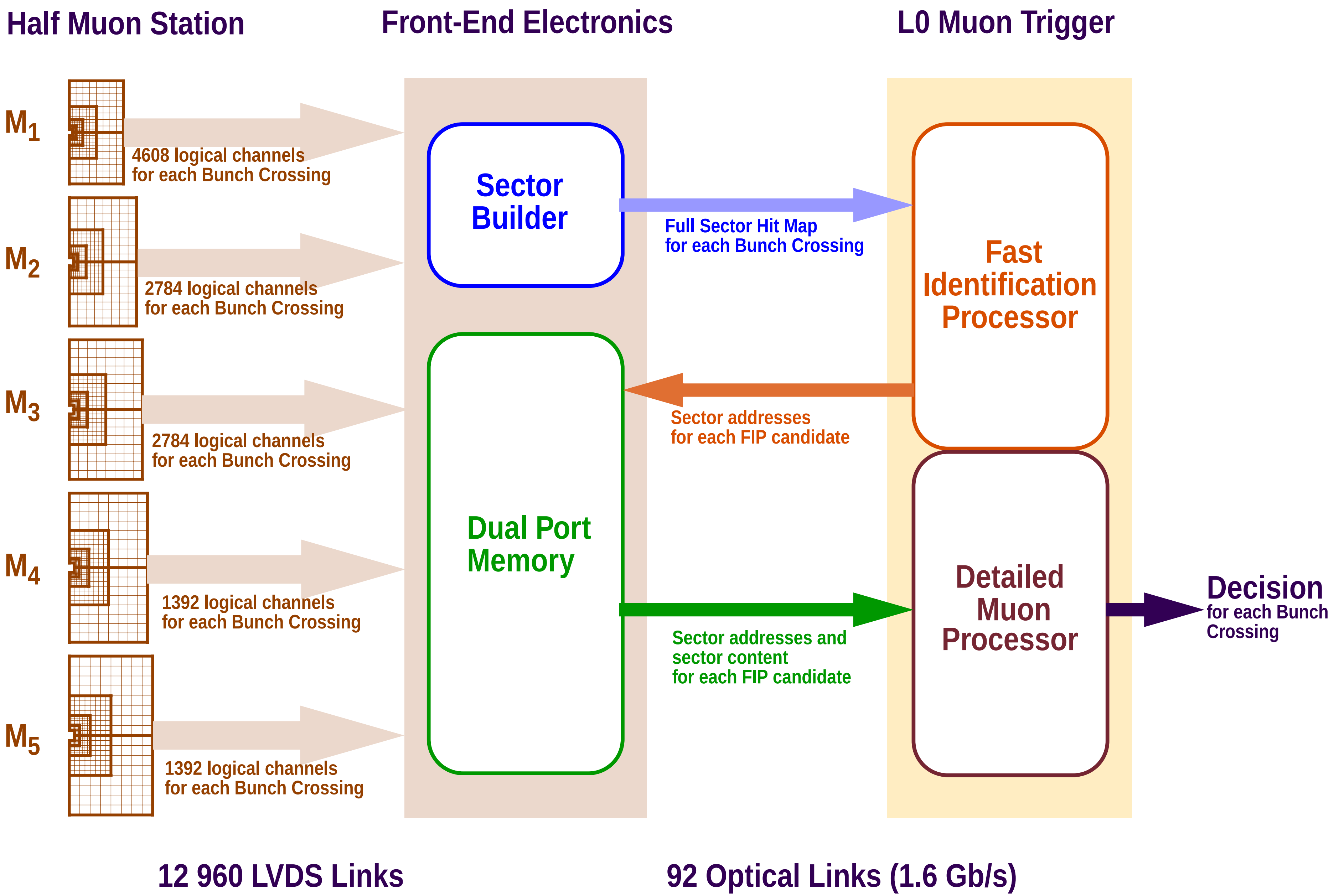
Robustness against background



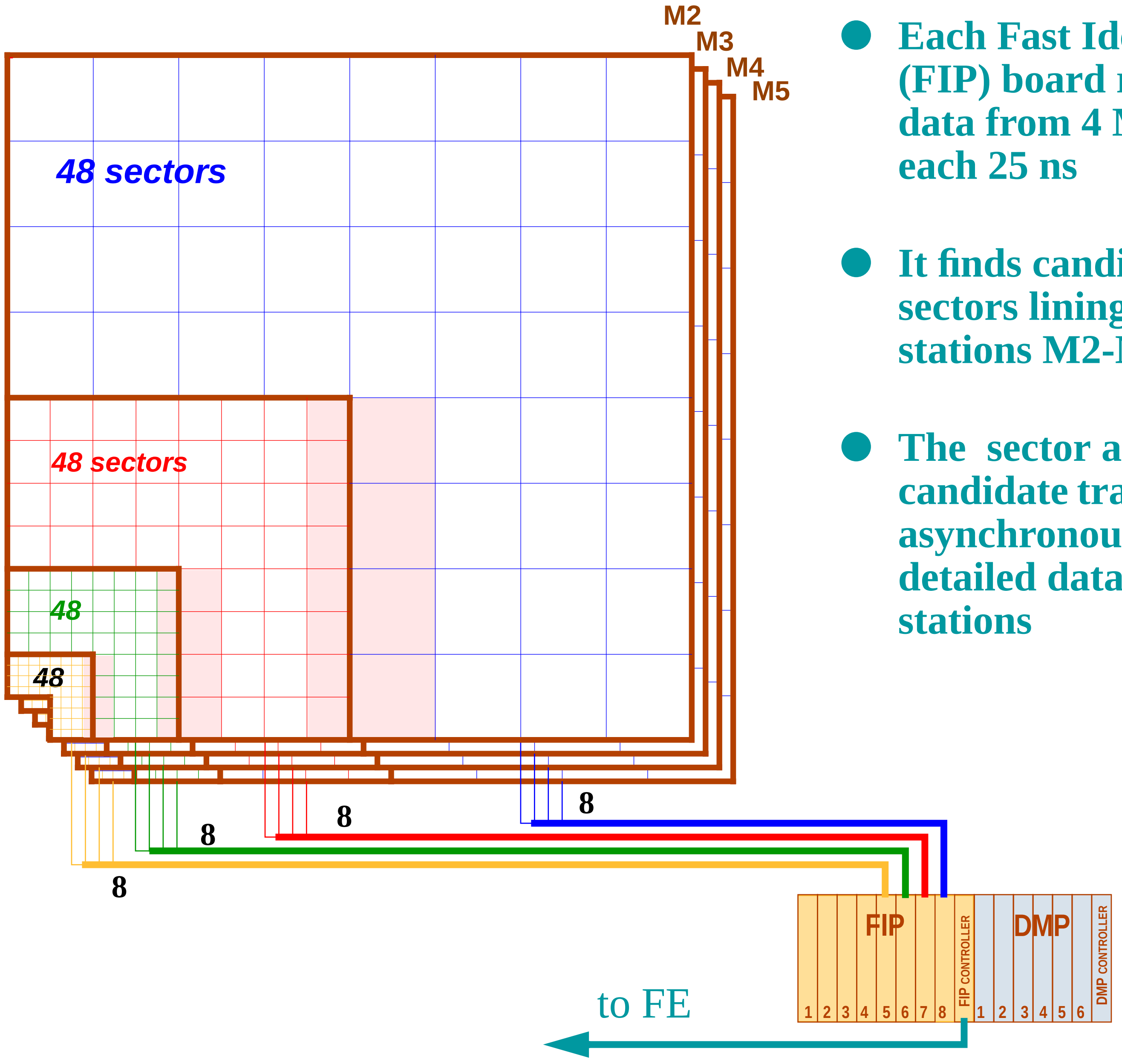
IMPLEMENTATION: REQUIREMENTS AND SOLUTION

- **Muon trigger processor implementation requirements:**
  - **minimal efficiency losses with respect to the “theoretical” algorithm**
  - **minimal amount of data transfer between the processor and the detector front-end electronics**
  - **fixed latency for taking a decision**
  - **easy to monitor and debug**
- **Specialised hardware processor**
  - **two independant processors for the right and left halves of the Muon System**
  - **two stages of the data processing**
    - **reduces the amount of data transfer by a factor of 10**

IMPLEMENTATION: GENERAL ARCHITECTURE



IMPLEMENTATION: FAST MUON IDENTIFICATION

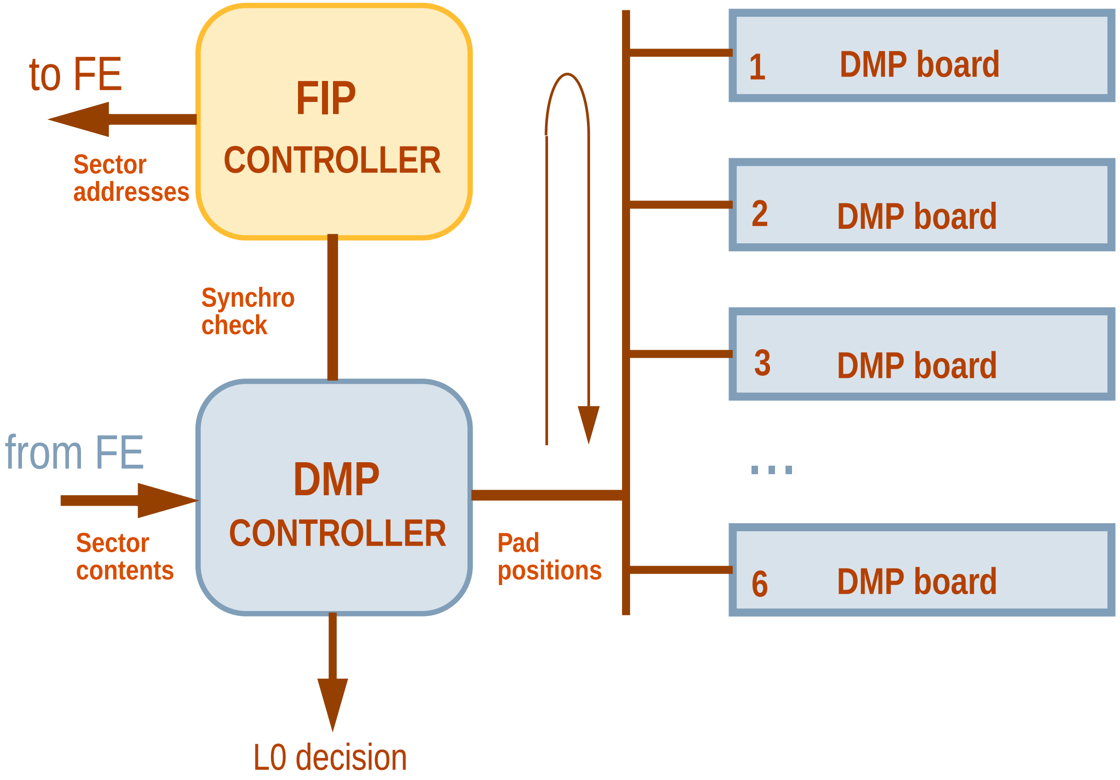


- Each Fast Identification Processor (FIP) board receives 48×4 sector data from 4 Muon stations M2-M5 each 25 ns

- It finds candidate tracks as a set of sectors lining up in all the 4 Muon stations M2-M5

- The sector addresses defining a candidate track are sent back to FE asynchronously for retrieval of the detailed data from all the 5 Muon stations

IMPLEMENTATION: DETAILED MUON PROCESSING



- Realizes theoretical algorithm in the area selected by the FIP processor
- Asynchronous processing of track candidates in DMP boards
- Results of the processing are collected by the DMP controller
- DMP controller restores the synchronisation before sending data to the L0 decision box

IMPLEMENTATION...

- **Latency**

Stage	Time [ns]
FIP Processor	200
ODE interrogation	300
DMP Processor	700
Total	1200

- **Logistics**
  - ➥ **2 VME64 crates on the sides of the Muon System**
  - ➥ **32 9U VME64 boards**
  - ➥ **184 1.6 Gbit/s optical links**
  - ➥ **up to 12 optical links on a board**

IMPLEMENTATION: TECHNICAL CHALLENGES

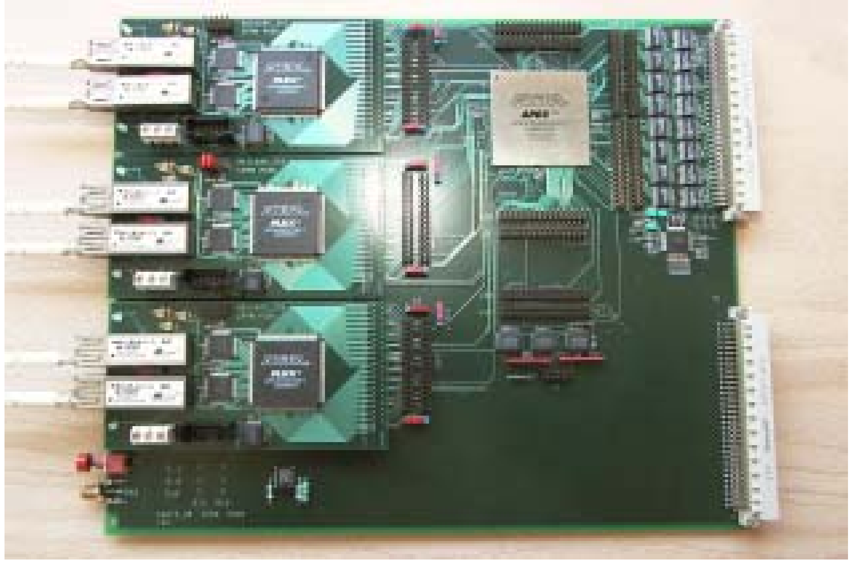
- **Large amounts of information to be received and processed in one board**
  - **using multiple optical links per board (up to 20)**
    - **data synchronization**
    - **low power consumption**
  - **using circuits of grand integration - very large FPGA's**

- **Transfer of large amounts of data inside the processor:**
  - **exchange of information between the cards:**
    point-to-point connection at up to 480 Mhz
  - **collection of data from multiple sources in one destination:**
    multipoint (up to 16) connection at 40 MHz

needs specialized backplane

- **Synchronisation of a large number of distributed devices**
  - **synchronisation protocols**

IMPLEMENTATION: TESTS



- 3 links at 1.6 Gbit/s are operational
  - ➥ several days of work without errors
  - ➥ synchronisation of 2 links with a time offset is demonstrated
- Large FPGA (ALTERA APEX400KE) is functional
  - ➥ 500 I/O channels
  - ➥ Ball Grid Array mounting technique
  - ➥ operation at 40 MHz
- Tests of a custom back planes are under preparation

CONCLUSIONS AND PROSPECTS

- **The performance of the L0 Muon Trigger processor is very close to the pure theoretical algorithm**